## ABSTRACT OF THE DISCLOSURE

A packet receiver includes a packet memory circuit for temporarily storing received packets in a FIFO (First-In First-Out) fashion in the form of a queue. A read start threshold setting circuit sets, with respect to the length of the queue, a read start threshold at which the received packets should begin to be read out. A read comparing circuit determines whether or not the length of the queue has reached the read start threshold, and outputs a read command signal in accordance with the result of decision. In response to the read command signal, a read control circuit causes the received packets to be read out of the packet memory circuit. The packet receiver reduces the influence of the jitter of a communication network on speech quality. Also, the packet receiver reduces the influence of delays of packets by executing discard processing with the queue.